ABSTRACT OF THE DISCLOSURE

A method for compensating for clock signal difference between a switch and peripheral device, including a receiving process and a transmitting process. For the receiving process, after an N-th packet is received, a first counter is triggered and begins to count. When an (N+1)-th packet is inputted, the counter stops counting and then an inter-packet gap IPG(N, N+1) between the N-th packet and the (N+1)-th packet is recorded into the N+1 queue link node QLN(N+1) according a counting value by the first counter; otherwise, the first counter keeps counting. For the transmitting process, after an inter-packet gap IPG(M-1, M) is obtained, and the M-th packet is transmitted, and then the second counter is triggered to begin to count. When a counted value by the second counter is equal to the clock cycle value corresponding to the inter-packet gap IPG(M-1, M), the second counter stops counting. When an inter-packet gap IPG(M, M+1) is obtained, and the (M+1)-th packet is then transmitted; otherwise, the second counter keeps counting.

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